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IN THE CLAIMS

1. (Currently amended) A frequency divider comprising: an input terminal ~~(4; 32)~~ for receiving a clock signal whose frequency is to be divided, an output terminal ~~(6; 34)~~ for outputting a frequency divided clock signal, wherein the frequency divider comprises: a shift register ~~(8; 36)~~ having cells ~~(10-13; 40-47)~~ for storing each bit of an initial word, said cells being series connected in a loop ~~(14; 48)~~, and said shift register being capable of shifting each bit of the initial word from the cell in which it is stored to the next cell in the loop at a rate clocked by the received clock signal, ~~and~~ wherein the output terminal ~~(6; 34)~~ is connected to the output of one cell of the loop of series-connected cells, and wherein the cells used in the loop of the shift register are selectable in either one of a first and a second group of cells, each cell of the first group always being initialized with a logic one, and each cell of the second group always being initialized with a logic zero.

2. (Currently amended) The frequency divider according to claim 1, wherein the number of cells connected in series in the loop is adjustable, and wherein the frequency divider comprises a control unit ~~(38)~~ to adjust this number of cells in order to achieve a desired frequency divider ratio.

3. (Currently amended) The frequency divider according to claim 2, wherein said shift register comprises at least one multiplexer ~~(54; 56)~~ to adjust the number of cells in the loop.

4. (Currently amended) The frequency divider according to claim 3, wherein each input

of ~~the or~~ each multiplexer is connected to the output of a respective cell of a group of series-connected cells, and an output of ~~the or~~ each multiplexer is connected to a next cell in said loop, and wherein the control unit ~~(38)~~ is able to control said at least one multiplexer in order to select which input of the or each multiplexer is connected to its output.

5. (Currently amended) The frequency divider according to claim 1, ~~wherein the cells used in the loop of the shift register are selectable in either one of a first and a second group of cells, each cell of the first group always being initialized with a logic one, and each cell of the second group always being initialized with a logic zero, and~~ wherein the frequency divider comprises a control unit ~~(38)~~ to select the cells used in the loop of the shift register in either one of said first and second groups in order to achieve a desired duty cycle.

6. (Currently amended) The frequency divider according to claim 5, wherein the shift register comprises a first and a second multiplexer ~~(54; 56)~~ to select cells in either the first or the second group.

7. (Currently amended) The frequency divider according to claim 6, wherein the output of each cells of the first group is connected to respective inputs of the first multiplexer ~~(54)~~ and an output of the first multiplexer is connected to the input of one cell of the second group, and the output of each cell of the second group is connected to respective inputs of the second multiplexer ~~(56)~~ and an output of the second multiplexer is

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connected to the input of one cell of the first group, and wherein the control unit ~~(38)~~ is able to control the first and second multiplexers in order to select for each of them which input of the multiplexer is connected to its output according to the desired duty cycle.

8. (Previously presented) The frequency divider according to any one of the previous claims, wherein the cells are flip-flops.

9. (Canceled)

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